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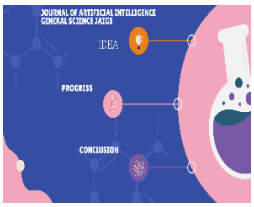

Novel Materials and Processes for Miniaturization in Semiconductor Packaging

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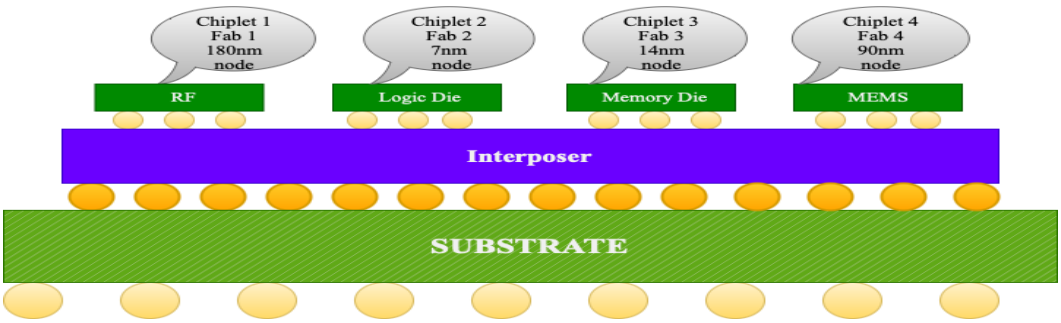
ABSTRACT

The semiconductor industry is undergoing a significant transformation away from conventional methods of shrinking devices and reducing costs. Chip designers are actively exploring new technological avenues to improve cost-effectiveness while integrating more features into the silicon footprint. One promising strategy is Heterogeneous Integration (HI), which employs advanced packaging techniques to integrate independently designed and manufactured components using the most suitable process technology. However, the adoption of HI brings about design and security challenges. To facilitate HI, it is crucial to advance research and development in advanced packaging.The existing research highlights potential security threats in the advanced packaging supply chain, particularly due to the offshore presence of most Outsourced Semiconductor Assembly and Test (OSAT) facilities/vendors. Addressing the growing demand for semiconductors and ensuring a secure semiconductor supply chain have prompted significant efforts from the United States (US) government to relocate semiconductor fabrication facilities onshore. However, enhancing US-based advanced packaging capabilities is essential to fully realize the vision of establishing a secure, efficient, and resilient semiconductor supply chain. Our endeavor was driven by the need to identify potential bottlenecks and vulnerabilities in the US-based advanced packaging supply chain.

Introduction

The pervasive integration of electronic devices is profoundly reshaping our daily lives and professional endeavors, becoming deeply ingrained in our routines. In today's digital-centric economy, the widespread utilization of high-speed devices and seamless connectivity generates a vast volume of data. Crucial systems such as autonomous vehicles, data centers, and Artificial Intelligence (AI) systems rely on capturing, storing, and analyzing this big data to facilitate data-driven transactions. Integrated Circuits (ICs) play a pivotal role in supporting the advancement of data processing, high-performance computing, and wireless communication. Modern ICs boast high-bandwidth memory, multiple processing cores, and high-speed input/output (I/O) ports. The development of these cutting-edge ICs can be largely attributed to Moore's Law, which has historically driven the semiconductor industry to produce faster, smaller, and more cost-effective ICs. However, Moore's Law faces limitations due to escalating fabrication costs, challenges in power dissipation, and yield issues associated with advanced technology nodes.

In response to the challenges encountered in the traditional scaling of CMOS technology, the International Technology Roadmap for Semiconductors (ITRS) 2015 introduced a forward-looking strategy to sustain the historical progress of CMOS technology. This strategy revolves around adopting Heterogeneous Integration (HI) as a viable solution. HI entails integrating individually designed and fabricated components on a substrate layer called an interposer, enabling them to function collectively as a System on Chip (SoC).



Heterogeneous Integration (HI) amalgamates separately manufactured components with varying technology nodes and functionalities, resulting in a more advanced assembly known as a Multi-Chip Module (MCM) or System in Package (SiP) (see Fig. 1). SiPs offer expanded functionality and improved operational characteristics that are difficult to accomplish with a single-die System on Chip (SoC) approach. Various components, including chiplets, active/passive parts, and MEMS devices, can be integrated into the SiP as a unified package. Chiplets, for instance, are individually fabricated silicon dies designed explicitly for targeted functions such as memory, analog-mixed signal processing, radio frequency (RF), or processors. The SiP integration can occur through adjacent placement (2.5D) or vertical stacking (3D) of chiplets on the interposer. While HI presents numerous advantages, further research and development are necessary to enhance its effectiveness. To realize the vision of HI and continue Moore’s Law,

packaging technology needs improvement to standardize interconnecting interfaces and communication protocols while ensuring secure design. For instance, packaging methods should efficiently utilize space to accommodate smaller form factors. Therefore, traditional legacy packaging technology proves insufficient to sustain HI and Moore's Law. Moreover, the design of interconnecting interfaces for chiplets must meet specific criteria for speed, power, and mitigating crosstalk issues. The influence of high-performance computing, 5G, and AI leads to amplified semiconductor speed, heightened interconnect density, reduced pad pitch, expanded chip size, and increased power dissipation. Thus, there is a need to assemble and stack chips and dies vertically to enable further scaling with faster interconnection, such as developing 2D, 2.5D, and 3D stacking. These factors pose challenges to continuing with traditional packaging technology, and significant research is ongoing to develop advanced packaging to cope with the requirements to realize HI.

Many key players in the semiconductor sector, including integrated device manufacturers (IDM) like Intel, Micron, and Samsung, fabless design firms such as IBM and AMD, foundries like TSMC and Samsung, as well as Outsourced Semiconductor Assembly and Test (OSAT) providers like Amkor and TSMC, are deeply involved in advancing HI solutions. For instance, commercially available examples of 3D SiPs include AMD EPYC and Intel Lakefield processors. The Defense Advanced Research Projects Agency (DARPA) shares a similar vision through its Common Heterogeneous Integration and IP Reuse Strategies (CHIPS) Program, aimed at advancing trusted microelectronics for the applications and technology requirements of the US Department of Defense (DoD). Despite efforts to bring chip fabrication onshore, it is essential to also develop onshore capabilities of advanced packaging in the US to fully secure the semiconductor supply chain. However, the US currently accounts for only 3% of the total advanced packaging market share, with the rest done offshore, which may compromise the semiconductor supply chain. Developing advanced packaging capabilities in the US is crucial to secure the semiconductor supply chain fully. Hence, each stage of the advanced packaging supply chain, as well as the major actors in each stage, requires critical examination to understand fully the current structure of the US-based advanced packaging ecosystem and identify potential bottlenecks that could threaten its stability and security.

In summary, we analyze the present state of the US-based advanced packaging ecosystem and propose countermeasures to mitigate hardware security issues posed by the current advanced packaging supply chain. Our contributions include analyzing onshore advanced packaging manufacturing capabilities, investigating dependencies of the US’s advanced packaging capabilities on offshore resources in various application sectors, providing an overview of current business development initiatives of semiconductor wafer manufacturing in the US, and identifying major requirements to develop a secure US-based advanced packaging supply chain.

This paper primarily analyzes the US-based advanced packaging supply chain ecosystem and its capabilities (see Fig. 2). The organization of the paper is as follows: Section II provides background and motivation for HI and advanced packaging. Section III introduces the US-based advanced packaging supply chain. Section IV examines economic and business development aspects of moving advanced packaging operations to the US. Section V presents a roadmap for securing an onshore US-based advanced packaging supply chain. Finally, Section VI concludes the paper.

Background

Motivation of HI

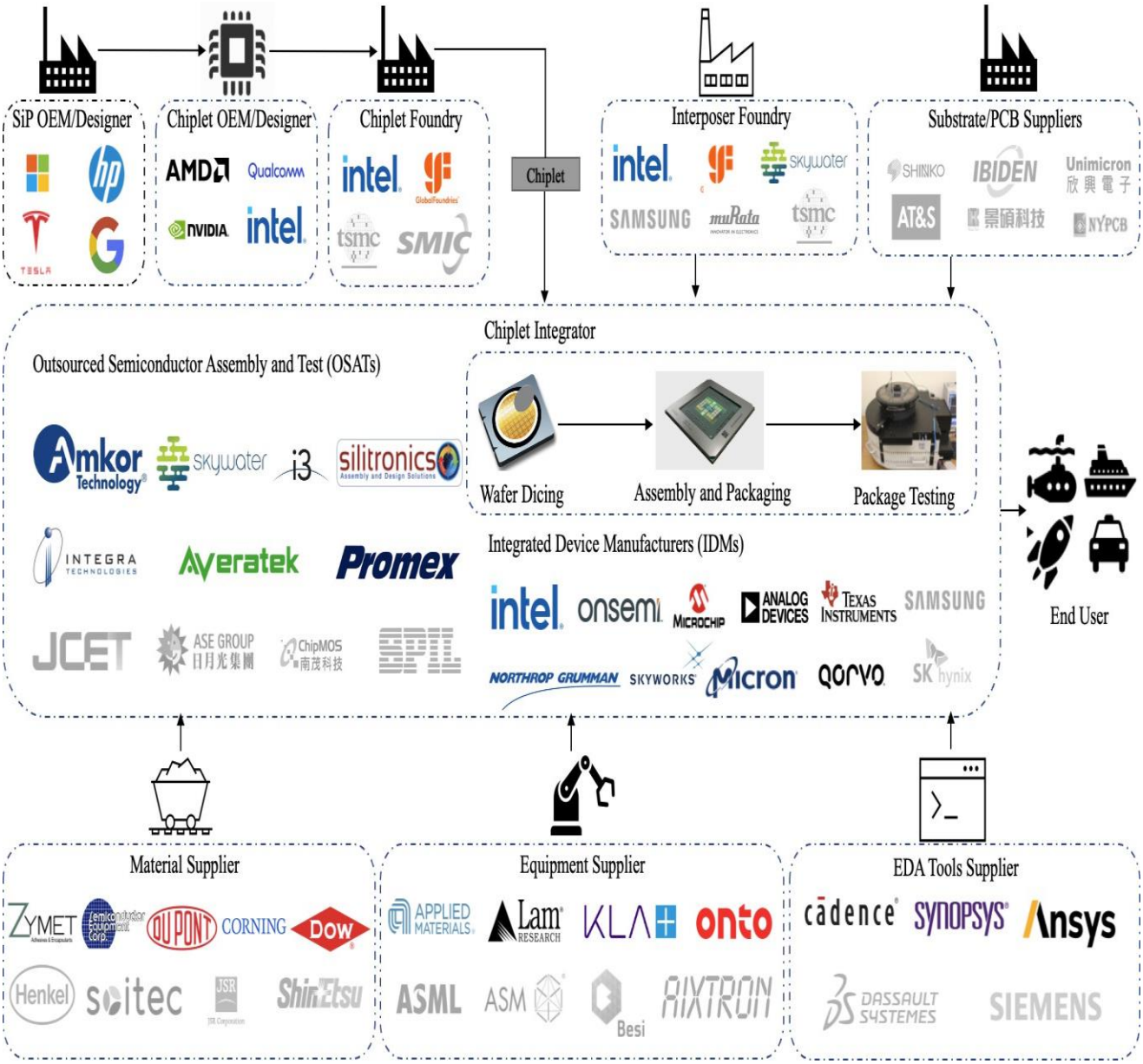
To keep pace with the continuation of More-than-Moore (MtM) progress, Heterogeneous Integration (HI) is essential. HI aims to increase performance and yield rate in smaller nodes, lower power consumption and semiconductor costs, and reduce latency among chiplets. The semiconductor industry actively pursues HI due to several significant drivers:

1) Characteristics of HI: DARPA identified three primary drivers for innovating in HI. Firstly, HI enables technological diversity by integrating chiplets from different technology nodes and foundries onto a common interposer. This allows for the combination of chiplets with varying technology levels, facilitating the integration of newer and older chiplets into the same package. Secondly, HI supports functional diversity by integrating chiplets with different functions onto a single package. This enables the design of System in Package (SiP) solutions that incorporate memory, logic, analog I/O, and MEMS sensor chiplets, allowing for modular and custom designs. Lastly, HI allows for materials diversity, meaning chiplets can be made from different materials as long as they do not adversely impact the system's functionality. This flexibility enables optimization of chiplets for specific functions and enhances capabilities using newer materials. Overall, HI promotes the integration of chiplets with diverse technologies, functions, and materials, leading to improvements in performance, cost-effectiveness, and design flexibility in semiconductor systems.

2) Continuance of Moore's Law: Moore's Law has been the cornerstone of innovation in the semiconductor industry for decades, propelling advancements by doubling transistor density in Integrated Circuits (IC) every two years. However, there is growing skepticism regarding the ongoing applicability of this law due to obstacles encountered in scaling transistor sizes (e.g., quantum phenomena) and escalating manufacturing expenses. Consequently, novel strategies like HI have emerged, fundamentally transforming packaging and design approaches. 3) Enhancing yield to achieve cost reduction: By integrating known good dies or chiplets with higher manufacturing yield, HI promises to enhance yield in SiP solutions. Technological advancements have played a role in improving integration and stacking yields while reducing manufacturing and research costs. Collective die-to-wafer bonding has been suggested to increase electrical die yields and transfer bonding. Moreover, utilizing chiplets from matured process nodes in SiP development reduces the necessity for post-silicon validation, leading to decreased development costs. Existing research shows promise of superior reliability and high yield in manufacturing high-performance 3D-ICs as well.

4) Minimizing form factor: Adopting 2.5D and 3D packaging techniques has resulted in smaller form factors and reduced size requirements. This size reduction is achieved by integrating multiple dies into a single package, eliminating the need for separate connections using traces on a Printed Circuit Board (PCB). As a result, the interconnections in these integrated technologies are smaller, leading to improved speed and lower power consumption. 2.5D packaging achieves a higher functional density than legacy packaging, where multiple dies are placed side by side on the top interposer. However, it falls short of the density achieved by 3D packaging in terms of functional density as it involves stacking dies vertically. However, it also poses challenges in managing thermal issues caused by the heat generated within the stacked dies. Therefore, using 2.5D and 3D packaging techniques in HI enables the realization of a compact form factor, enhanced performance, high manufacturing yields, and reduced overall area requirements of the chip.

5) Utilizing SiP technology to enhance performance: As the performance gains from increasing transistor density on a single-die approach plateaued, HI can continue Moore's Law by incorporating multiple dies in SiP. This integration presents an opportunity for higher performance through improved memory access speeds. For example, 3D packaging technology enables the stacking of CPU and memory dies, leading to enhanced memory bandwidth and reduced transmission latency thanks to shorter interconnects between the dies. Ongoing research is focused on improving the communication quality and interconnect in interposers. There are even proposals to introduce active interposers, which embed transistor-based logic circuits within the interposer itself, further enhancing the functional density of the SiP.



Advanced packaging to enable HI

The imperative of integrating multiple dies or chiplets within a single package underscores the critical role of advancing advanced packaging technologies, positioning semiconductor engineers and physicists at the forefront of their capabilities. The task of accommodating an increased number of silicon dies within a reduced footprint necessitates both vertical and horizontal stacking, entailing additional wire bonding, densely packed smaller bumps, heightened routing complexity, and potential interference from neighboring signal paths. Various packaging

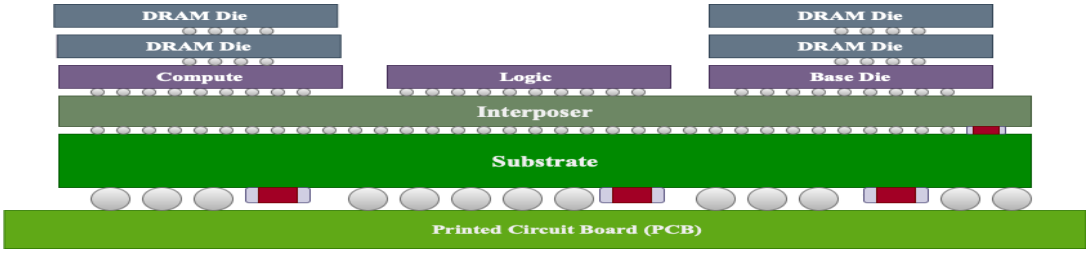
technologies have emerged to address these wide-ranging design challenges for advancing HI. Below are discussions of a few common packaging technologies:

1) Legacy packaging: Referring to traditional packaging methods widely employed, legacy packaging encompasses techniques such as dual in-line package (DIP), quad flat package (QFP), and small outline integrated circuit (SOIC). While legacy packaging has historically served the industry well, it comes with limitations in size, power dissipation, and signal integrity. However, it still finds application in specific areas, such as low-cost devices or applications with lower performance requirements.

2) Flip-Chip packaging: To enhance chip performance and efficiency while reducing interconnection distances, Flip-Chip Ball Grid Array (FCBGA)-based packaging has been developed. In this configuration, chips are either placed or antennas are formed on the surface of the package, while digital, analog, or Radio Frequency (RF) ICs are monolithically integrated into the bottom of the ball grid array substrate. This approach enables improved power efficiency and high data rates, albeit with thermal management challenges. Micro-bumps are introduced to enhance connectivity and reduce parasitism.

3) Wafer Level Packaging (WLP): WLP, a standard chip packaging approach, employs thin metal layers to create redistribution layers (RDL). Fan-out wafer-level packaging (FOWLP) has emerged as a popular method for mmWave microelectronics packaging, offering benefits such as size and thickness reduction, enhanced RF performance, and greater design flexibility. However, warpage poses a significant challenge in FOWLP, addressed through technologies like embedded Wafer Level Ball Grid Array (eWLB) for high-volume production at reasonable costs.

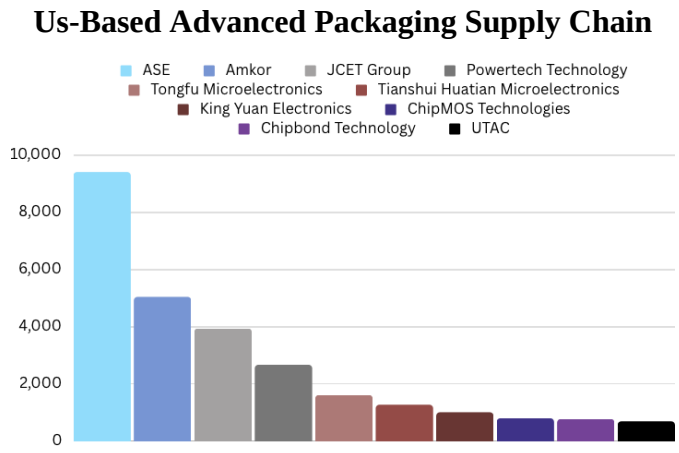
4) 2.5D Packaging: In 2.5D packaging, a separate interposer layer is positioned between the chiplets and the packaging substrate. Primarily focusing on integrating cutting-edge logic and memory elements within a single package, 2.5D packaging facilitates high-speed data communication between these devices. A notable example is Chip-on-Wafer-on-Substrate (CoWoS) developed by TSMC, where multiple chiplets or dies are stacked atop a silicon interposer, attached to a substrate using micropumps or through-silicon vias (TSVs). Initially, chips are bonded to the interposer using flip-chip or wire bonding techniques, followed by attachment to a substrate. The chip-facing side of the interposer typically comprises multiple.



Metal layers or RDL facilitate the distribution of electrical signals from the I/O pads on the chiplets to their corresponding pads on the silicon interposer. Interposer-based 2.5D packaging proves particularly valuable when integrating dissimilar chiplets, such as memory, processors, and MEMS-based sensors. Various companies have developed their own 2.5D packaging solutions, encompassing memory, processors, and MEMS-based sensors. Diverse materials, including IBM's direct bonded heterogeneous integration (DBHi), TSMC's local silicon interconnect (LSI), and ASE's stacked Si bridge fan-out chip-on-substrate (sFO CoS), have also been employed to create interposers.

Another approach to 2.5D packaging involves using "bridges" to establish connections between adjacent chips. Embedded Multi-die Interconnect Bridge (EMIB) serves as an example of bridge-based 2.5D packaging. In this method, the bridge is fabricated separately and embedded within the cavity of the packaging substrate. Some literature categorizes this bridge-based advanced packaging solution as a 2.3D packaging structure. Silicon blocks with high I/O density are employed to create these "bridges," facilitating interconnections between chiplets positioned in close proximity to each other. Companies are actively exploring developing their own bridge solutions due to the cost-effectiveness of this approach compared to interposer-based 2.5D packaging.

3D packaging technology enables stacking and interconnection of semiconductor dies by placing one on top of another, typically employing vertical connections known as TSVs. This approach is commonly used to stack memory atop a processor or to integrate analog and digital circuits. Intel's Foveros stands as a prime example of 3D packaging technologies, which is a type of Die-on-Die (DoD) packaging. In DoD packaging, distinct functional dies are stacked using TSVs and micro-bumps to establish electrical connections between the layers. Another form of 3D packaging is Package-on-Package (PoP), which typically involves vertically connecting two packaged dies and linking them through package vias (TPV). PoP technology finds extensive application in imaging sensors and chips used in portable devices.



With the introduction of the CHIPS (Creating Helpful Incentives to Produce Semiconductors) Act, the US government has expressed its desire and commitment to bring semiconductor wafer fabrication facilities onshore. However, to fully secure the entire semiconductor supply chain, back-end operations cannot be ignored. Therefore, it is crucial to pay equal attention to developing advanced packaging capacity onshore as well. A critical examination of the existing packaging capacity in the US reveals that there is sufficient capacity for legacy packaging. Thus, developing Outsourced Semiconductor Assembly and Test (OSAT) facilities with advanced packaging capabilities makes more sense. However, with merely a 3% market share in the global market, the US lags in advanced packaging capacity. Hence, ramping up the advanced packaging manufacturing capabilities in the US is important. To realize the vision of a healthy, burgeoning domestic advanced packaging supply chain, it's important to first examine the current structure of the advanced packaging ecosystem, capabilities, off-shore dependency, and potential weaknesses in the US.

1) SiP OEM/Designer: Original Equipment Manufacturer (OEM) refers to a company that designs and manufactures products or components used in another company's end product. SiP designers or OEMs either set specifications for their SiP according to their needs or directly procure the SiP from the chiplet designer. For example, Microsoft buys chips from chiplet designers like AMD, NVIDIA, or Intel for their data centers. On the other hand, Tesla may design a SiP and outsource them to a chiplet OEM for fabrication or procure chips directly from Intel, AMD, and Texas Instruments for their autonomous vehicles.

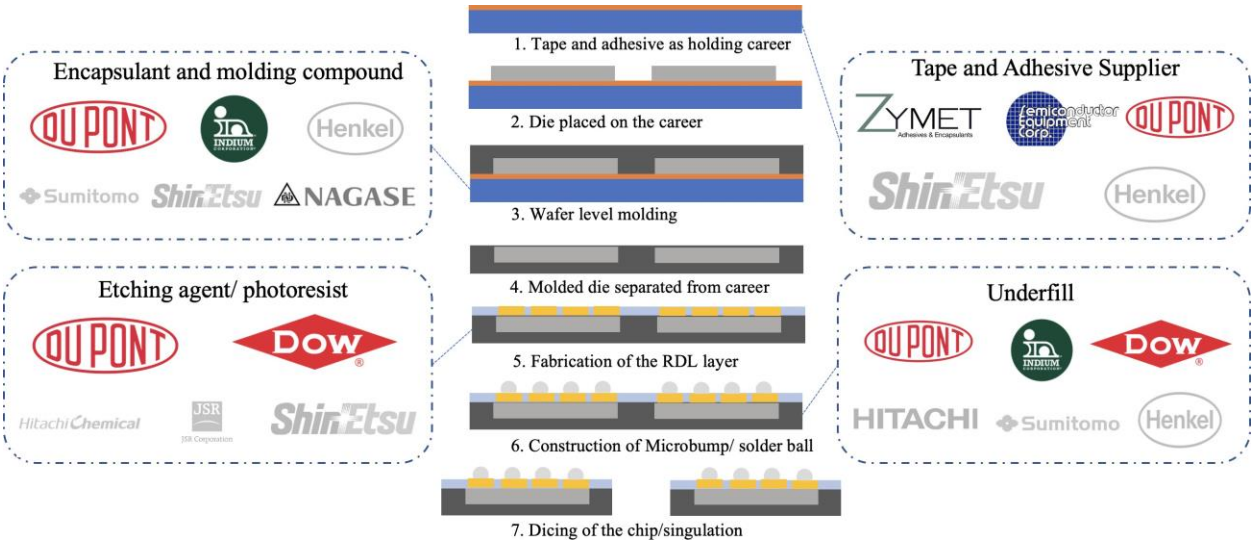
2) Chiplet OEM/Designer and Chiplet Foundry: A chiplet designer designs the chiplet for the SiP OEM/designer. The chiplet designer may have a fab or be fabless. In the latter case, a fabless chiplet designer outsources chip fabrication to an onshore or offshore Chiplet Foundry for fabrication. AMD, NVIDIA, Apple, Qualcomm, and Broadcom are prime examples of fabless chiplet designers which do not have manufacturing capabilities. For example, AMD, Apple, and NVIDIA outsource chip fabrication to TSMC, an offshore Chiplet Foundry. AMD works closely with TSMC, ASE, and Tongfu Microelectronics for advanced packaging capabilities, such as 2.5D packaging. Apple entirely depends on TSMC for chip fabrication and advanced packaging capabilities. AMD and NVIDIA datacenter's GPU depend on TSMC for their CoWoS packaging technology. Other prominent Chiplet Foundries are GlobalFoundries, Samsung, SMIC, UMC, etc., which provide chip fabrication services for the fabless chip designer. Due to the current geopolitical tensions between China and Taiwan, the world semiconductor supply chain is severely vulnerable to potential geopolitical turmoil. Such a conflict would affect leading semiconductor companies, such as AMD, NVIDIA, and Qualcomm, among others, as TSMC accounts for 56% of the total semiconductor market share in the world. Hence, more investment is needed in the US to secure chip production and/or advanced packaging capacity for fabless American chip designers.

3) Chiplet Integrator: A chiplet integrator can either be a single entity offering comprehensive integration services, including interposer design, packaging, assembly, and testing, or it can be divided into multiple separate entities, depending on its expertise or business model. There are primarily two classes of chip integrators: Integrated Device Manufacturers (IDMs) and OSAT vendors. While an IDM has end-to-end chip design, fabrication, and packaging capabilities, an OSAT vendor only provides packaging design and manufacturing capabilities. In the US, a few companies, such as Intel, Qorvo, Texas Instrument, and Onsemi, are qualified as IDMs. For instance, Intel developed the 3D stacking with Foveros technology. Similarly, Qorvo offers advanced packaging capabilities, like an Antenna in Package (AiP), essential in wireless communication. Additionally, Micron is dedicated to memory technologies and related advanced packaging capabilities. Finally, Northrop Grumman and Honeywell are IDMs dedicated to the defense and aerospace sectors. There are currently 25 OSAT vendors in the US, but not all can offer advanced packaging capabilities. The most well-known US-based OSAT vendor is Amkor, but Amkor does not have any manufacturing capabilities in the US. Promex is building onshore advanced packaging capabilities. Sitronics has advanced packaging capabilities, offering a Multi-Chip Module (MCM) platform with a buildup substrate and doesn't use silicon interposer technology. Skywater is building fab and packaging facilities to offer advanced packaging capabilities. The US has always been a leader in developing cutting-edge semiconductor technologies, including packaging. However, more investment is needed to ramp up onshore advanced packaging operations' design and manufacturing capabilities.

4) Material Supplier: Semiconductor advanced packaging requires complex manufacturing and process flow, which consists of various stages like dicing and slicing the wafer, placing it into the mold and wire bonding, stacking the chiplet, or encapsulating the chiplet. In different stages of the process flow, various raw materials are required. Dielectric materials, leadframe, gold wire, encapsulant, and molding compound

5) Equipment Suppliers: Various types of equipment are used in different stages of packaging manufacturing, such as dicing, wire-bonding, microbump, and hybrid bonding. In Wafer Level Packaging (WLP), the wafer needs to be diced, and then the Redistribution Layer (RDL) is formed on top of the wafer. This step requires conventional

photolithography equipment used for chip fabrication. Flip chip bonding equipment attaches the IC chips directly onto the substrate or Printed Circuit Board (PCB) by accurately positioning and bonding the solder bumps on the chip to the corresponding pads on the substrate, allowing for high-density interconnections. Wire bonding equipment connects the IC chip to the substrate or PCB using fine wires made of gold, aluminum, or copper. It connects the wires from the chip's bond pads to the appropriate bonding pads on the substrate, enabling electrical connectivity. Die attach machines place and bond the IC chips onto the substrate or PCB. They use adhesive materials, such as epoxy or solder, to secure the chip in the desired location. Molding equipment is used in encapsulation, where a protective package is formed around the IC chip. This equipment encloses the chip in a plastic or ceramic material, providing mechanical protection and environmental isolation. Various testing and inspection equipment are used to verify the functionality and quality of the packaged ICs. This includes Automated Optical Inspection (AOI) systems, X-ray inspection machines, electrical testers, and other specialized testing tools. Wafer dicing machines cut the processed silicon wafers into individual IC chips. They utilize mechanical or laser cutting techniques to dice the wafer into the desired chip sizes. Applied Materials and Lam Research are prime examples of US-based equipment suppliers for the semiconductor industry and advanced packaging. Besides this, KLA, Onto Innovation, Nordson, Thermofisher Scientific, and Bruker provide various equipment for metrology needs. US companies provide necessary inspection and metrology tools for all stages in the manufacturing process.



Requirements and Capabilities of US-based Advanced Packaging Supply Chain across Various Sectors

In the upcoming sections, we will assess the existing and future capabilities of US companies to produce and integrate technologies utilizing Heterogeneous Integration (HI) and advanced packaging. These evaluations aim to pinpoint critical areas in the US advanced packaging technology market that may require support beyond domestic manufacturing capacities alone.

To conduct these evaluations effectively, we will outline specific needs for each technological domain, evaluate the capacity of US Outsourced Semiconductor Assembly and Test (OSAT) providers in deploying advanced packaging methods for each domain, identify the reliance of US technology sectors on foreign OSATs for manufacturing, and conduct a security assessment for each of these technological domains (Refer to Table I, Table II). The following sections will analyze the advanced packaging capabilities and dependencies within various application fields, such as Defense and Aerospace, 5G and Communications, High-Performance Technologies, Automotive, Internet of Things, Mobile, Medical, and Health.

1) Defense and Aerospace: The Defense and Aerospace (A-D) sector faces unique challenges necessitating HI, including the assurance of high reliability and durability in packaging, and the establishment of a secure domestic supply chain (Refer to Table I). To address these needs, the US has 83 trusted suppliers with onshore manufacturing facilities, crucial for safeguarding the semiconductor supply chain for the US defense industry. These suppliers, classified as DoD Tier 1 trusted suppliers, encompass fabrication facilities, OSATs, Integrated Device Manufacturers (IDM), SiP designers, among others. For instance, companies like Qorvo specialize in semiconductor manufacturing for both consumer and defense markets, providing Application-Specific Integrated Circuits (ASIC), Radio Frequency Integrated Circuits (RFIC), and communication chips for RADAR applications. These companies conduct design, fabrication, manufacturing, and packaging operations in secure US-based facilities to ensure maximum security and reliability for defense industry requirements. Moreover, prominent defense companies like Raytheon, Honeywell, and Northrop Grumman possess IDM status along with advanced packaging capabilities within the US, ensuring the fulfillment of defense industry needs. Hence, the US exhibits substantial onshore capabilities in the A-D sector to meet demand.

2) 5G Communications: The rapid expansion of 5G technology in smartphones and Internet of Things (IoT) systems has amplified data traffic and the need for accelerated data transmission (Refer to Table I). High-frequency applications of 5G networking, particularly relevant for mmWave 5G, demand advanced packaging solutions like Antenna-in-Package (AiP) for beamforming. AiP integration enables the embedding of a beamforming antenna array within the package itself, ensuring smaller device footprints and shorter interconnections between RFICs and antennas. While a few US companies like Qorvo, Skyworks Solutions, and Analog Devices develop essential chips and packaging for 5G applications, only a subset, such as Qorvo and Skyworks Solutions, possess onshore AiP manufacturing capabilities. Additionally, companies like Infineon and Renesas, although having onshore foundries,

are based in Europe. The dependency on foreign manufacturers is notable, especially for high-frequency applications, potentially impacting the US 5G market.

3) High-Performance Computing: Advanced packaging requirements in high-performance applications prioritize optimal performance, reliability, and efficiency (Refer to Table I). In the US, companies like Intel, AMD, and NVIDIA are key suppliers of high-performance chips. While Intel, as an IDM, can manufacture 2.5D/3D stacked chips onshore, its semiconductor process node technology lags behind offshore foundries like TSMC and Samsung. Fabless companies like AMD and NVIDIA rely entirely on offshore fabs for advanced process nodes up to 5nm. The increasing demand for Application-Specific Integrated Circuits (ASICs) for machine learning workloads and Field-Programmable Gate Arrays (FPGAs) necessitates reliance on offshore foundries like TSMC for fabrication. Moreover, critical components for supercomputing and data center applications, such as Network Interface Cards (NICs), primarily supplied by Mellanox Technology, are manufactured offshore. The geopolitical tensions between China and Taiwan pose potential risks to the semiconductor industry, especially in high-performance computing applications. While TSMC and Samsung are establishing onshore fabs to meet demand, further investment in onshore IDM and OSAT facilities is essential to fully secure the high-performance computing sector in the US.

4) Automotive: Advanced packaging requirements in automotive applications emphasize crucial factors such as high reliability, longer product life cycles, and sensor integration (Refer to Table I). During the late 2020s, as the automotive market began to recover, suppliers faced challenges in restoring production capacity, a task proven to be arduous. The majority of automotive ICs utilize wire-bond packages such as SOIC, TSSOP, QFN, QFP, BGA, and Power Discrete. According to Yole, approximately 90% of packaging for automotive applications involves lead or laminate substrates. Shortages in substrate supply contributed to the automotive chip scarcity. Additionally, for high-performance processors in autonomous vehicles handling AI workloads, there's a requirement for 2.5D and 3D packaging. These processors exhibit an offshore dependency on manufacturers like TSMC and Samsung. AiP is crucial for mmWave RADAR, a primary sensing modality for autonomous vehicles. Overseas entities like Valeo, Robosense, and Livox dominate the majority of the LiDAR supply, while Velodyne, a US-based LiDAR supplier, holds only a 3% market share. However, significant offshore dependency persists for LiDAR and RADAR packaging, as Amkor, the sole US-based OSAT providing packaging solutions for the automotive sector, lacks onshore manufacturing capabilities. Addressing this significant offshore dependency is crucial to secure the US-based automotive chip ecosystem.

5) Internet of Things (IoT): With projections indicating over 500 billion devices connected to the Internet by 2030, the IoT necessitates more heterogeneous systems to advance these applications (Refer to Table I). Vital requirements for packaging solutions in IoT include low cost per unit, power efficiency, small form factor, and sensor integration. This advancement aims to further connect various devices globally, enhancing daily life convenience. IoT devices find applications in medical and health, wearables, edge AI, autonomous vehicles, and more. AiP is essential for 5G connectivity in IoT applications, while the fan-out package is widely adopted for edge AI applications in IoT devices, enabling high-density connections in packaging. FOWLP is commonly used for small form factor packaging in IoT devices. The medical sector extensively utilizes IoT, detecting metabolites to diagnose health issues rapidly. Diverse packaging technologies for IoT applications exhibit significant offshore dependency, necessitating attention.

6) Mobile: The mobile sector serves as a major catalyst for electronics innovation, representing a significant portion of the global electronics market and used by a vast percentage of the world's population (Refer to Table I). Sensor integration, low power consumption, small form factor, and efficient thermal management are primary considerations in designing packaging solutions for mobile applications. PoP architecture or WLP is typically employed for the SoC in mobile devices, while stacked architecture is used for memory chips. High-end smartphones widely adopt PoP packaging due to their ability to meet demanding I/O and performance requirements. SiP technology is prevalent for

sensors and RF chips in mobile devices. Qualcomm and Apple dominate as mobile SoC providers in the US, yet they rely entirely on TSMC for fabricating their SoCs and packaging solutions. Skyworks Solution or Broadcom may provide sensors or communication chips. Skyworks, an IDM, operates from the US. However, the heavy reliance on TSMC or Samsung for mobile SoCs poses significant security risks in the supply chain.

7) Medical and Health: The medical and health sectors represent critical application fields for semiconductor chips, utilized in various implants, sensors, medical instruments, and machinery (Refer to Table I). Miniaturization, biodegradability, and superior electrical performance are key requirements for packaging solutions in medical and health applications. Various substrate materials are used in medical electronics, including ceramic substrates like LTCC, flexible circuits, and laminate substrates.

Application fields	Advanced packaging requirements
Aerospace and Defense	- High reliability, durability, and long product life cycle in the extreme environment - Secure domestic supply chain and leverage verification technologies to safeguard data and system security - High-performance design for ensuring a competitive edge
5G Communication	- Enabling beamforming by embedding antenna in the package for mmWave communication - Low noise, interference, minimizing cross-talk between circuitry - Power efficiency in mobile 5G applications - High-Frequency operation - Considering temperature issues generated from the high-frequency operation
High-Performance Computing	- High-speed interconnects in packaging to enable high-speed data transfer between chiplets - Integrating heat spreaders, heat sinks, and thermal interface materials to ensure heat dissipation - Optimizing power distribution, minimizing power losses, and efficient power power delivery - Increasing testability and yield by stacking multiple chiplets - Vertical stacking of memory and compute die for low latency, high-speed data transmission
Automotive	- High reliability, longer product lifecycle in an extreme environment such as vibration and extreme temperature - Integrating sensors such as MEMS, LiDAR, and RADAR in a single package - High-performance computing for autonomous vehicles
Internet of Things (IoT)	- Low power consumption - Small form factor - Ensuring low cost per unit - Various sensor integration - RF performance for 5G applications
Mobile	- Integration of various functionalities, such as processor, memory, sensors, and wireless communication modules - Low power consumption and high-speed data transfer - Efficient thermal management and heat dissipation - Ensuring a small form factor is essential
Medical and Health	- Excellent electrical performance to ensure accurate data transmission, signal integrity, and power delivery - Miniaturation and small form factor while maintaining optimal performance - Hermetic sealing to prevent contamination while using in a sterile environment - Ensuring biocompatibility for safe medical applications - Reliability, durability, and long life cycle - Flexible packaging technology for wearable medical devices

Emerging packaging and manufacturing technology

1) Additive manufacturing for advanced packaging: Additive manufacturing, also known as 3D printing, revolutionizes the manufacturing process by building three-dimensional objects layer by layer. Unlike traditional subtractive methods like cutting or machining, additive manufacturing starts with a digital 3D model and adds material to create the physical object. Recently, there's been a growing trend towards using additive manufacturing in semiconductor advanced packaging, offering several advantages such as flexibility, miniaturization, cost-effectiveness, and rapid prototyping with diverse materials. The capability to print intricate features and structures at a micron scale enables the development of highly integrated packages, aligning with the semiconductor industry's trend towards miniaturization. Rapid prototyping facilitates quick testing of newly developed packaging designs and technologies.

Leading US-based companies in additive manufacturing for advanced packaging include Averatek and Optomec. Averatek's A-SAP technology enables direct printing of circuits on various flexible substrates, eliminating the need for traditional etching processes and enabling the production of complex circuitry with fine-line widths and tight geometries. Optomec offers additive manufacturing solutions for Wafer-Level Packaging (WLP), high-frequency RF interconnects in packaging, and shielding. Given the advantages of additive manufacturing in semiconductor packaging, the US needs to bolster this sector to meet future demand.

2) Silicon photonics: Silicon photonics, an advanced technology gaining significant attention, leverages silicon-based materials to manipulate light, enabling the integration of photonic and electronic components on a single chip. This integration offers numerous advantages, particularly in Heterogeneous Integration (HI).

A key advantage of silicon photonics in HI lies in its ability to provide fast data rates and wide bandwidth capabilities. Traditional IC packaging faces challenges in connecting multiple devices efficiently, but silicon photonics offers extremely fast data rates and wide bandwidth, enabling efficient and high-speed communication between devices. Through 3-D stacked packaging, interconnects are significantly shortened, reducing latency delays. Additionally, integrating photonics with other components on a single chip allows for space-efficient designs.

US-based companies excelling in silicon photonics include AIM Photonics and Atomica, dedicated to related packaging technologies empowering optical communications, 3D sensing, LiDAR, augmented/virtual reality (AR/VR), thermal imaging, illumination, and various optical sensing applications.

Economics of Advanced Packaging: Nationally vs. Globally

The CHIPS and Science Act of 2022 aims to bolster the American semiconductor industry and uphold US leadership in designing and developing technology solutions across various sectors, including defense and aerospace, 5G and communications, automotive, mobile, medical, health applications, high-performance computing, and IoT systems, as elaborated in Section III-A. This act allocated a total of $52.7 billion to the Department of Commerce, Department of Defense, Department of State, and National Science Foundation to advance the American semiconductor industry through research, development, manufacturing, and workforce development initiatives. Out of this allocation, $39 billion is earmarked for manufacturing incentives, while $13.2 billion is dedicated to research, development, and workforce training. Additionally, the bill established the International Technology and Security Innovation (ITSI) Fund, providing $0.5 billion to promote secure and trustworthy information and communication technologies and to establish secure and resilient global semiconductor manufacturing supply chains worldwide.

To realize the objectives outlined in The CHIPS and Science Act, the CHIPS Program Office announced plans to invest in leading-edge logic devices, advanced packaging, leading-edge memory devices, and current-generation and mature-node semiconductors. Recognizing the industry's differentiation between conventional and advanced packaging, the CHIPS Program Office has devised distinct strategies for each. While reshoring conventional packaging operations in an economically competitive manner poses challenges, the focus will be on shifting conventional packaging activities from countries of concern to US allies and partners to ensure sufficient and secure global conventional packaging capacity for the US. Conversely, to cultivate a robust advanced packaging capacity domestically, multiple high-volume advanced packaging facilities will be established within the US, aiming to establish the country as a global technology leader in commercial-scale advanced packaging for logic and memory devices.

The reconfiguration of global conventional packaging operations and the development of domestic advanced packaging operations, along with their potential impact on buyer and supplier relationships in the underlying supply chains, can be understood using the concept of value chains. A value chain comprises operations needed to design, manufacture, and deliver a finished product to a customer, with a lead firm driving value addition and distribution, and a set of supplier firms providing necessary know-how and capabilities. Different types of value chains exist, including local, regional, and global. Local value chains connect lead firms and suppliers within a single country, regional value chains connect those within a single world region, and global value chains connect lead firms with globally dispersed supplier firms.

Today, most complex products, including semiconductor products, are built using global value chains. The practice of segmenting value chains into different stages and seeking optimal locations and supply modes for each stage has led to the relocation of substantial portions of value chains from developed economies to emerging economies. Consequently, most manufacturing and packaging operations in the semiconductor industry are located outside the US today. Moreover, some production processes are segmented to the extent that products may cross international borders numerous times before reaching end customers. For instance, a single chip may undergo over 1,000 processing steps and cross international borders more than 70 times before reaching its final destination.

conclusion

In conclusion, the research on novel materials and processes for miniaturization in semiconductor packaging underscores the critical role of innovation in advancing the semiconductor industry. Through the exploration of emerging technologies such as additive manufacturing, silicon photonics, and advanced packaging techniques, significant strides have been made towards achieving miniaturization, enhancing performance, and meeting the demands of diverse application fields.

The integration of additive manufacturing offers promising avenues for flexible, cost-effective, and rapid prototyping solutions in semiconductor packaging. Companies like Averatek and Optomec are spearheading this revolution, enabling the direct printing of circuits and the development of complex packaging designs with fine-line widths.

Similarly, silicon photonics presents exciting opportunities for revolutionizing data communication systems, particularly in the context of heterogeneous integration. AIM Photonics and Atomica are driving advancements in this domain, offering integrated photonic and electronic components on single chips to deliver fast data rates, wide bandwidth capabilities, and efficient space utilization.

Furthermore, the emphasis on advanced packaging techniques, as outlined in initiatives like the CHIPS and Science Act of 2022, signals a concerted effort to strengthen the semiconductor industry domestically. By investing in leading-edge logic devices, advanced packaging, and memory technologies, the US aims to secure its position as a global technology leader while addressing supply chain vulnerabilities and reshoring conventional packaging operations.

Overall, the research underscores the importance of collaboration, innovation, and strategic investment in advancing semiconductor packaging technologies. As the industry continues to evolve, embracing novel materials and processes will be essential for driving miniaturization, enhancing performance, and meeting the growing demands of diverse application fields in the digital era.

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